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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/887,560	06/25/2001	Edward Colles Nevill	550-243	7549

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EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 12/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/887,560	NEVILL ET AL.	
	Examiner	Art Unit	
	Aimee J Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 September 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9 and 12-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 12-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-17 have been examined. Claims 1-9 and 12-17 have been amended as per Applicant's request. Claims 10-11 and 18-20 have been cancelled as per Applicant's request.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed on record in the file: Amendment as received on 15 September 2004.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-9 and 12-17 are rejected under 35 U.S.C. 102(e) as being anticipated by Patel et al., U.S. Patent No. 6,332,215.

5. Regarding claim 1, Patel has taught an apparatus for processing data, said apparatus comprising:

a. A processor core (26 of Fig.1) having a register bank (48 of Fig.3) containing a plurality of registers and being operable to execute operations upon register operands held in said registers as specified within instructions of a first instruction set (see Col.4 lines 46-54),

b. An instruction translator (42 of Fig.3) operable to translate instructions of a second instruction set into translator output signals corresponding to instructions

of said first instruction set (see Col.4 lines 1-4), instructions of said second instruction set specifying operations to be executed upon stack operands held in a stack (see Col.2 lines 19-21),

c. Wherein said instruction translator is operable to allocate a set of registers within said register bank to hold stack operands from a portion of said stack (see Col.4 lines 46-54 and Col.6 lines 1-11),

d. Said instruction translator has a plurality of mapping states in which different registers within said set of registers hold respective stack operands from different positions within said portion of said stack (see Col.4 lines 6-22 and Col.5 line 48 – Col.6 line 11).

e. Said instruction translator is operable to change between mapping states in dependence upon operations that add or remove stack operands held within said set of registers (see Col.4 lines 6-22 and Col.5 line 48 – Col.6 line 11).

f. Wherein said instruction translator uses a plurality of instruction templates (78 of Fig.4) for translating instructions from said second instruction set to instructions from said first instruction set (see Col.5 lines 30-42).

g. Wherein an instruction from said second instruction set including one or more stack operands has an instruction template comprising one or more instructions from said first instruction set in which register operands are mapped to said stack operands in dependence upon a currently adopted mapping state of said instruction translator (see Col.5 lines 30-60).

6. Regarding claim 2, Patel has taught an apparatus as claimed in claim 1, wherein said translator output signals include signals forming an instruction of said first instruction set (see Col.4 lines 1-4).

7. Regarding claim 3, Patel has taught an apparatus as claimed in claim 1, wherein said translator output signals include control signals that control operation of said processor core and said control signals match control signals produced on decoding instructions of said first instruction set (see Col.2 line 65 – Col.3 line 5). Here, native instructions, which are control signals that control the processing core, are the same whether they were translated from Java bytecodes or not when being passed to the processor core (see Fig. 3).

8. Regarding claim 4, Patel has taught an apparatus as claimed in claim 1, wherein said translator output signals include control signals that control operation of said processor core and specify parameters not specified by control signals produced on decoding instructions of said first instruction set (see Col. 5 lines 43-47). Here, non-translated instructions will not access the instruction translator (see Fig.3), and thus will not produce output to the Java Registers (44 of Fig.4).

9. Regarding claim 5, Patel has taught an apparatus as claimed in claim 1, wherein said instruction translator provides mapping states such that stack operands are added to or removed from said set of registers without moving stack operands between registers within said set of registers (see Col.5 line 48 – Col.6 line 11).

10. Regarding claim 6, Patel has taught an apparatus as claimed in claim 1, wherein said set of registers are operable to hold stack operands from a top portion of said stack including a top of stack operand form a top position within said stack (see Col.4 lines 6-22).

11. Regarding claim 7, Patel has taught an apparatus as claimed in claim 1, wherein said stack further comprises a plurality of addressable memory locations holding stack operands (see Col.4 lines 12-15).

12. Regarding claim 8, Patel has taught an apparatus as claimed in claim 7, wherein stack operands overflow from said set of registers into said plurality of addressable memory locations (see Col.4 lines 54-60 and Col.6 lines 1-24).

13. Regarding claim 9, Patel has taught an apparatus as claimed in claim 7, wherein stack operands held within said plurality of addressable memory locations are loaded into said set of registers prior to use (see Col.4 lines 54-60 and Col.6 lines 1-24).

14. Regarding claim 12, Patel has taught an apparatus as claimed in claim 1, wherein said instruction translator comprises one or more of:

a. Hardware translation logic (42 of Fig.3),

b. Instruction interpreting program code controlling a computer apparatus,

c. Instruction compiling program code controlling a computer apparatus,

d. Hardware compiling logic.

15. Because the claim is written in the alternative format, only one of the four possible alternatives has to be met, and thus Patel has taught the limitations of the claim.

16. Regarding claim 13, Patel has taught an apparatus as claimed in claim 1, wherein said instruction translator includes a first plurality of state bits indicative of a number of stack operands held within said set of registers (see Col.5 lines 34-47). Here, there are counters that keep track of the number of entries on the stack (see Col.5 lines 34-37), and the stack is held in

the set of registers with the translator keeping track of the arrangement of the stack in the registers (see Col.5 lines 43-47).

17. Regarding claim 14, Patel has taught an apparatus as claimed in claim 13, wherein said instruction translator includes a second plurality of state bits indicative of which register within said set of registers holds said top of stack operand (see Col.4 lines 6-22).

18. Regarding claim 15, Patel has taught an apparatus as claimed in claim 1, wherein said second instruction set is a Java Virtual Machine Instruction set (see Col.2 lines 60-63).

19. Regarding claim 16, Patel has taught a method of processing data using a processor core (26 of Fig.1) having a register bank (48 of Fig.3) of containing a plurality of registers and being operable to execute operations upon register operands held in said registers as specified within instructions of a first instruction set (see Col.4 lines 46-54) using a plurality of instruction templates (Col.5 lines 30-42 and 78 of Fig.4), said method comprising the steps of:

a. Translating instructions of a second instruction set into translator output signals corresponding to instructions of said first instruction set (see Col.4 lines 1-4), instructions of said second instruction set specifying operations to be executed upon stack operands held in a stack (see Col.2 lines 19-21),

b. Allocating a set of registers within said register bank to hold stack operands from a portion of said stack (see Col.4 lines 46-54 and Col.6 lines 1-11),

c. Adopting one of a plurality of mapping states in which different registers within said set of registers hold respective stack operands from different positions within said portion of said stack (see Col.4 lines 6-22 and Col.5 line 48 – Col.6 line 11) wherein an instruction from said second instruction set including at least one stack

operand has an instruction template comprising at least one instruction from said first instruction set in which register operands are mapped to said stack operands in dependence upon a currently adopted mapping state of said translating step (see Col.5 lines 30-60)

d. Changing between said plurality of mapping states in dependence upon operations that add or remove stack operands held within said set of registers (see Col.4 lines 6-22 and Col.5 line 48 – Col.6 line 11).

20. Regarding claim 17, Patel has taught a computer readable medium including computer readable instructions that when executed perform the method of claim 16 (see Col.2 line 65 – Col.3 line 5 and the above rejection for claim 16).

Response to Arguments

21. Examiner withdraws objections to the abstract in favor of the amended abstract.

22. Examiner withdraws objection to claim 17.

23. Examiner withdraws objections under subsection 8a, 8b, and 8c in the last Office Action, dated 30 June 2004, in favor of the amended claims.

24. Examiner withdraws objections under subsection 8d in the last Office Action, dated 30 June 2004.

25. Examiner withdraws 35 USC § 112 (second paragraph) to claim 3 in favor of the amended claim.

26. Applicant's arguments filed 15 September 2004 have been fully considered but they are not persuasive. Applicant argues in essence on pages 13-14

However, there appears to be no disclosure in the Patel reference suggesting that an instruction template which is associated with an instruction from the second (non-native) instruction set has an instruction set comprising "one or more instructions from said first instruction set" (the native instruction set) wherein "register operands are mapped to said stack operands in dependence upon a currently adopted mapping state of said instruction translator."

27. This has not been found persuasive. Patel in column 5, lines 30-60, specifically lines 48-60, describes the translation of Java bytecode to native instruction code of an example instruction. Patel teaches that the Java bytecode, in its Java virtual machine is executed via stack operations using stack operands, but, when translated into native instruction, becomes register operations using register operands. Therefore, register operands are mapped to stack operands when translating from native to non-native.

Conclusion

28. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

29. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

30. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:30am-5:00pm.

31. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

32. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

RICHARD L. ELLIS
PRIMARY EXAMINER

AJL
Aimee J. Li
14 December 2004